AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A digital signal processor comprising:

an instruction memory, a central arithmetic unit, a register, a controller, an event control unit and input/output devices;

the instruction memory is arranged to include one or more operation codes including logical operations, time performance constraints and events;

the controllers is arranged to initiate operation of the event control unit in response to one of the one or more operation codes, suspend all further processing ~~by the controller~~ of ~~operation codes~~ the time performance constraints after initiating operations in an event control unit and resume processing ~~by the controller~~ of the time performance constraints when advised by the event control unit; and

the event control unit is arranged to recognize an event and in response to the detection of the event execute a processing operation and initiate or resume processing of the controller upon completion of the processing operation, wherein the event is an input signal or a completion of processing from a previous event and the operation code comprises an event operand arranged to identify the input signal or previous event to initiate or resume processing of the event control unit and a delay operand comprising those time performance constraints executed by a counter in the event control unit.~~;~~

~~wherein the event control unit includes a package controller, a buffer register operable to store operands of a pulse package associated with a current operation code and an active register operable to store the operands of a pulse package associated with the previous operation code wherein the package controller controls the transfer of operands to the buffer register and from the buffer register to the active buffer.~~

2. (Previously presented) A digital signal processor in accordance with claim 1, wherein the event is detected by the event control unit.

3. (Previously presented) A digital signal processor in accordance with claim 2, wherein the event control unit is arranged to detect input signals.

4. (Previously presented) A digital signal processor in accordance with claim 2, wherein a further event is recognized as a completion of the processing carried out as a consequence of the event.

5. (Previously presented) A digital signal processor in accordance with claim 1, wherein the event is recognized as a completion of the processing carried out as a consequence of a previous event.

6. (Previously presented) A digital signal processor in accordance with claim 1, wherein the event control unit includes a signal memory arranged to store and extract data under control of the event control unit.

7. (Previously presented) A digital signal processor in accordance with claim 6, wherein the signal memory is a vector memory.

Claims 8 and 9 (Cancelled)

10. (Previously presented) A digital signal processor in accordance with claim 1, including two ore more event control units arranged to work independently from each other.